4

Paper #4

SHEET 1 OF 1

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. ARC.015A	APPLICATION NO. 09/808,469
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	APPLICANT Peter Warnes	
	FILING DATE March 14, 2001	GROUP 2123

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
MV	1	5,463,746	10/31/95	Brodnax, et al.			
MV	2	5,748,650	05/05/98	Blaker, et al.			
MV	3	5,764,994	06/09/98	David John Craft			
MV	4	5,794,010	08/11/98	Worrell, et al.			
MV	5	5,867,681	02/02/99	Worrell, et al.			
MV	6	5,896,519	04/20/99	Frank Worrell			
MV	7	5,901,310	05/04/99	Rahman, et al.			
MV	8	5,905,893	05/18/99	Frank Worrell			
MV	9	6,195,743	02/27/01	Elmootazbellah Elnozahy			
MV	10	6,233,674	05/15/01	Elmootazbellah Elnozahy			
MV	11	6,237,080	05/22/01	Rauno Makinen			
MV	12	6,263,429	07/17/01	Charles P. Siska			
MV	13	6,268,809	07/31/01	Akira Saito			
MV	14	6,275,921	08/14/01	Iwata, et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

EXAMINER INITIAL		**OTHER DOCUMENTS** (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
MV	15	Lefugry, Charles, et al. (1999) "Evaluation of a High Performance Code Compression Method," IEEE - Proceedings of Micro 32 (consisting of 10 pages).
MV	16	Application Serial No. 09/418,663 entitled "Method and Apparatus for Managing the Configuration and Functionality of a Semiconductor Design," filed October 14, 1999 – Attorney Docket No. ARC.001A

EXAMINER	DATE CONSIDERED 4.19.04

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

Paper #5

SHEET 1 OF 1

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. ARC.015A COPY OF PAPERS ORIGINALLY FILED	APPLICATION NO. 09/808,469
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	APPLICANT Peter Warnes	
	FILING DATE March 14, 2001	GROUP 2123

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
MK	17	5,819,058	10/06/98	Miller, et al.			
MK	18	5,848,255	12/08/98	Yoshikazu Kondo			

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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
MK	19	EP 0 843 253 A1	May 1998	Europe				
MK	20	WO 00/29938	May 2000	PCT				

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

EXAMINER	DATE CONSIDERED 4.19.2004

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	APPLICATION NO.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	ARC.015A	09/808,469
	APPLICANT Peter Warnes	COPY OF PAPERS ORIGINALLY FILED
	FILING DATE March 14, 2001	GROUP ~~2123~~

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
MH	21	5,812,416	09/22/98	Gupte, et al.			
MH	22	5,884,057	03/16/99	Blomgren, et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
MH	23	EP 1 050 798 A1	May 1999	Europe				

EXAMINER INITIAL		**OTHER DOCUMENTS** (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
MH	24	Berekovic, et al., (Oct. 1998), "A Core Generator for Fully Synthesizable and Highly Parameterizable RISC-Cores for System-On-Chip Designs," IEEE Workshop on Signal Processing Systems. SIPS. Design and Implementation, Pages 561-568, XP002137267
MH	25	Karl Guttag (March 1983), "µP's on-chip macrocode extends instruction set," Electronic Design, Vol. 31, No. 5, Pages 157-161
MH	26	Dolle, et al., (July 1997), "A 32-b RISC/DSP Microprocessor with Reduced Complexity," IEEE Journal of Solid-State Circuits, IEEE Inc., New York, Vol. 32, No. 7, Pages 1056-1066, XP000729365

EXAMINER	DATE CONSIDERED 4.19.2004

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